Partitioning Trends in Chip Design

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Emerging Market Drivers are Analog Intensive

A few years ago, industry watchers predicted that the analog market would suffer as the world turned towards digital. However, the analog market has grown steadily over the past few years. In 2004, the analog market totaled $31 billion and is expected to grow to $37.5 billion in 2006. As the market transitions from personal computers (one per person) to consumer electronics (many per person), the need for more sophisticated analog chips is increasing. Most emerging markets, such as ultra wideband, digital video broadcast, WiMAX, 802.11n, etc., require complex analog and radio frequency (RF) functions to support digital functions. Future semiconductor growth drivers, such as portable, wireless and multimedia, are analog intensive.

Partitioning Approaches

The integration of analog functionality on a digital chip becomes an intense debate during the chip architecture phase for emerging analog-intensive products. In the last few years, few companies have been able to create a complete system on a single chip. For example, consider a digital subscriber line (DSL) client-side modem. Its constituent blocks include a line driver, an analog baseband (ABB) (includes analog filters, data converters and gain amplifiers), a digital baseband (DBB) (includes digital filters, memories and processor) and a power management subsystem (PMU). If one were to adopt a traditional approach in partitioning this chip, each of these subsystems would be designed using the best-suited IC process technology. For example, the line driver would be designed using a high-voltage, high-speed BiCMOS technology; the ABB would be designed using a 0.35-micron (or similar) analog CMOS technology; the DBB would be designed using a deep-submicron (DSM) digital CMOS technology (130-nanometer and 90-nanometer); and the PMU would be designed using a high-voltage technology. A system-on-chip (SOC) approach would be to design all of the blocks mentioned using a DSM digital CMOS technology, so the entire DSL modem can be realized in a single chip.

The situation is similar in a cell phone system. Figure 1 shows the various subsystems that constitute a cell phone system, along with the process technology that best suits each of these subsystems.

Figure 1. Technologies in a Cell Phone

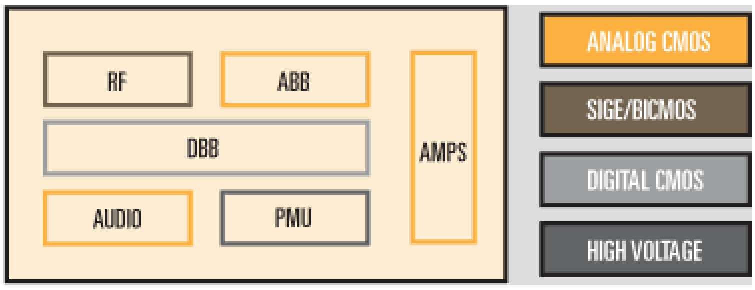
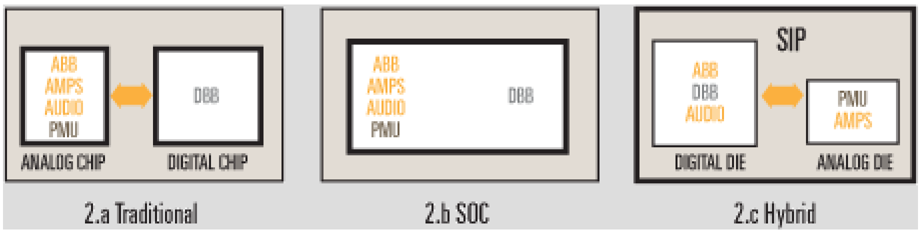


Figure 2 shows three different approaches to the problem of partition: (a) traditional approach, (b) SOC approach and (c) hybrid approach. The remainder of this article will investigate the relative merits and demerits of each approach and will explain how adopting the hybrid approach can combine the merits of the traditional and SOC approach.

Figure 2. Traditional, SOC and Hybrid Approaches



Factors Used to Determine Chip Partition

The following factors are used in determining chip partition:

- Footprint (total space occupied by the packages in the board)
- Cost
- Power
- Time-to-Market
- Development Cost

The degree of importance of each factor varies for different applications. For example, cost is of highest importance and form factor (decided by the footprint) is of lowest importance for wallpowered applications, such as broadband modems. On the other hand, for a cell phone solution, form factor (handheld device) and power (long battery life) will be as important as the cost of the entire solution. The relative performance of the proposed approaches is considered in the following sections. For the purpose of simplicity, RF design is not considered in the analysis.

Traditional and SOC Approaches

As mentioned earlier, with the traditional approach one would design each subsystem using the best-suited IC process technology. An analog chip design requires high-quality passives and robust transistor models. As a result, the analog chip would typically be designed using an analog friendly process technology, such as 0.35- micron CMOS with some high-voltage features, while the digital chip would be designed using a DSM process, such as 0.13- micron/90-nanometer CMOS.

The SOC approach is integrating all (or most of) the functions required for the system in a single substrate. Complex analog, high-voltage power management and all digital functions are integrated using a DSM process, such as 0.13-micron or 90-nanometer. Merits and demerits of each approach are described below.

Power – Analog blocks, such as audio and ABB, are not very power effective when using high-geometry analog CMOS technology. The interface between analog and digital chips also consumes power; therefore, the traditional approach becomes less attractive than the SOC approach when looking at power consumption.

Footprint – The footprint is usually higher when using the traditional approach since it involves more than one package, and analog blocks, such as audio and ABB, are not effective if developed in a higher geometry process (more silicon area). System-in-a-package (SiP) techniques can be effective and are used to improve the footprint. However, the improvement obtained is not significant enough to match its SOC counterpart. SiP is having multiple dies in a single package.

Cost – Package cost is higher when using the traditional approach since it involves more than one package. However, certain analog design does not scale in silicon area with technology. For example, silicon area might not differ from 0.35-micron to 0.13- micron or 90-nanometer technology for a certain class of analog designs. Producing all the analog designs in an expensive DSM process offsets the cost benefit associated with the elimination of a package. Hence, cost would be neutral for both approaches.

Time-to-Market – Analog designs usually undergo a couple revisions to get the silicon fully functional and parametric. Electronic design automation (EDA) tools used in analog designs are not sophisticated enough to accurately predict the performance of the silicon. Accuracy of the transistor model is important to achieve parametric success. Designing analog circuits in 0.35-micron, where the transistor models are more robust, offers a greater chance of success than generating the designs in a DSM process, such as 90- nanometer. In addition, issues, such as substrate noise coupling (noise generated from the switching of digital circuits that can deteriorate the sensitive analog signals), are not present when using the traditional approach. Hence, development time is usually faster with the traditional approach than with the SOC approach.

Development Cost – Most silicon is revised after being shipped to a customer for a period, either to improve yield or to improve various performance parameters. Even if the designs are validated through shuttle, one should expect a few revisions to improve yield or analog performance. A typical mask set for a 90-nanometer design can run approximately $1 million. If the design requires revisions because of analog integration issues, etc., the development cost could be significantly higher. On the other hand, a typical mask set for a 0.35-micron design can run approximately $40,000; therefore, the development cost will be lower when using the traditional approach.

Overall, the traditional approach is very effective in terms of development cost and time-to-market, neutral with respect to cost, and less effective with respect to footprint and power. The SOC approach is very effective in terms of power and footprint, neutral with respect to cost, and less effective with respect to development cost and time-to-market.

Hybrid Approach

The hybrid approach is aimed at combining the merits of both the traditional and SOC approach. Instead of assuming that everything should be in a single substrate (SOC approach) or all analog functions should be in an analog chip (traditional approach), the hybrid approach determines chip partition using the following guideline.

The chip architect prioritizes the key factors that affect chip partition for the intended application. As mentioned previously, these factors include footprint, power, cost, time-to-market and development cost. The hybrid approach requires two silicon die – one using DSM technology, such as 0.13-micron or 90-nanometer, and another using analog CMOS technology, such as 0.35-micron, with high-voltage capability.

Every block in the system is then analyzed to determine whether it needs to be developed using a DSM process or an analog CMOS technology to achieve the priority that was assigned earlier. SiP is considered for reducing the footprint. Figure 2.c describes the partition.

Analog blocks, which are low in power and boast an effective die area in a DSM process, are created using a DSM process, while PMU and AMPS blocks (class D speaker drivers for audio) are created using an analog CMOS process with high-voltage capability. This partition also addresses the reliability issues of high-voltage analog functions in a SOC chip. For example, a battery voltage of 4.2V or a USB voltage of 5.5V can be handled in analog die.

Most would agree that a product family serves most markets. Using the SOC approach, it would be expensive to create a family of chips using a DSM process. However, when using the hybrid approach, blocks, which can change because of different customer needs, can be created in the analog CMOS die. With this approach, there could be a single DSM die and several companion analog die that could be fabricated economically, meeting the different customer needs. For example, in the cell phone system previously mentioned, there are PMU blocks (different types of batteries, power rating, etc.) and AMPS blocks (speaker drivers with different power ratings). By being part of the analog die, different analog dies can be created cost effectively and meet different customer needs.

Power – Analog blocks effective in power in DSM technology are created using a DSM process; therefore, power will be closer to that of the SOC approach. Correct partitioning can minimize the power resulting from the interface between digital and analog.

Footprint – Analog blocks effective in silicon area in DSM technology are created using a DSM process; therefore, the total silicon area is closer to that of the SOC approach. With SiP, the difference between the SOC and hybrid approach is minimal.

Cost – This approach should be attractive in terms of cost (low power and small footprint). The hybrid approach can be more cost efficient than the SOC approach.

Development Cost – The development cost of the hybrid approach is similar to the development cost of the traditional approach. Analog blocks that are better suited for design in DSM technology are created using a DSM process, while blocks that demand high-quality passives and high-voltage tolerance are created using an analog CMOS technology. As explained earlier, this approach offers a cost-effective method to create a product family, meeting the needs of multiple customers.

Time-to-Market – When using this approach, time-to-market is similar to the traditional approach since placing the sensitive analog circuits in the analog die reduces the issues of substrate noise coupling, etc.

The hybrid approach is effective in terms of power, footprint, cost, development cost and time-to-market. This approach is a better choice for partitioning in a wide variety of applications.

Conclusion

Table 1 is a comparison of the three approaches. As illustrated in the table, the hybrid approach is effective across all factors of chip partitioning. This could result in a new business model for analog companies, where bare silicon dies, rather than packaged devices, are sold. The hybrid approach, along with SiP, may possibly help companies overcome the current challenges of higher development cost and faster time-to-market.

Table 1. Comparison of the Three Approaches

	Power	Cost	Footprint	Dev Cost	Time-to-Market
Traditional	Less Effective	Neutral	Less Effective	Very Effective	Very Effective
SOC	Very Effective	Neutral	Very Effective	Less Effective	Less Effective
Third	Effective	Effective	Effective	Effective	Effective

Very Effective · Less Effective · Effective · Neutral

About the Author

Ganapathy Subramaniam co-founded Cosmic Circuits in 2005. Cosmic Circuits focuses on analog IP. Prior to Cosmic Circuits, Ganapathy worked at Texas Instruments for 16 years in various capacities, such as director of the mixed-signal technology center at Texas Instruments India and worldwide silicon development manager for WLAN.