

### KEY FEATURES

- Low-area and low-power clock-generation PLL with low jitter, and high VCO frequency, suitable for a variety of applications
- Long-term jitter (accumulated rms): 40pS
- Maximum Period jitter (peak-peak) : +/- 2% of output clock period
- Supports a wide-range of input frequencies from 3 MHz- 200MHz suitable for consumer and communication applications
- High VCO frequency of 300-1000MHz provides flexibility in input and output frequency combinations
- High PSRR: tolerates up to 50 mV p-p noise on I/O supply and 30 mV p-p noise on core supply
- Power Supply
  - I/O supply of 1.62 – 3.6V
  - Core supply of 1.2V± 10%
- Core Cell Area: Contact [ip@cosmiccircuits.com](mailto:ip@cosmiccircuits.com)
- Low-power: Contact [ip@cosmiccircuits.com](mailto:ip@cosmiccircuits.com)
- TSMC 65nm 1P6M LP process, with 2.5V IO MOS with 3.3V OD

### OVERVIEW

CC0310INPLL-T65LP is ideal for generating system clocks and interface clocks at a low accumulated RMS jitter of 40pS and a period jitter of +/-2%. Its low period-jitter makes it suitable for systems implementing high-speed data-transfers, system clocking and interfaces. Its high VCO frequency of 1.0 GHz makes it versatile in supporting a variety of input frequencies. The programmable output dividers along with the high VCO frequency give us flexibility in deriving many output frequencies.

### DIFFERENTIATION

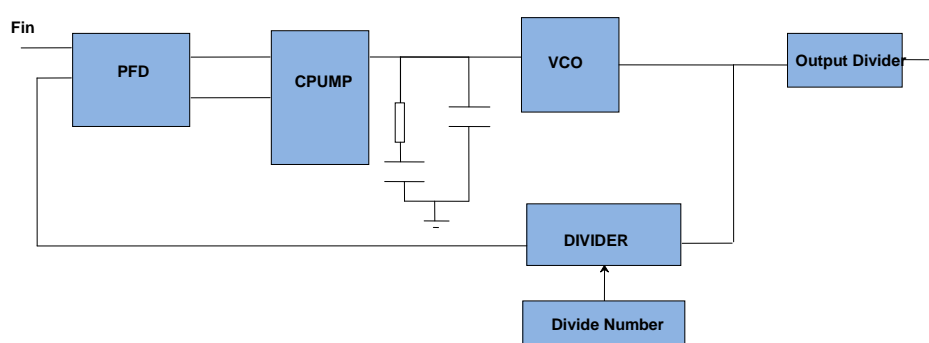
- Highly compact
- Low-power suitable for battery-powered applications
- Supports a wide power supply range

These have been achieved even while the VCO up to 1GHz and a low reference frequency down to 3MHz, while retaining flexible programmability, making the PLL versatile for multiple applications.

### APPLICATIONS

- System-clocking
- Interface clocking
- Battery powered applications

### BLOCK DIAGRAM



### SPECIFICATIONS TABLE

| Parameter                          |       | Condition                             | Value  |     |      | Units              |
|------------------------------------|-------|---------------------------------------|--|-----|------|--------------------|
|                                    |       |                                       | Min  | Nom | Max  |                    |
| Power Supply                       | VDD33 |                                       | 1.62   | 3   | 3.6  | V                  |
|                                    | VDD12 |                                       | 1.08   | 1.2 | 1.32 | V                  |
| Temperature                        |       |                                       | -40  |     | 125  | C                  |
| Input Frequency                    |       |                                       | 3  |     | 200  | MHz                |
| Input division                     |       |                                       | 1  |     | 32   | Counts             |
| Divider Reference frequency        |       |                                       | 3  |     | 50   | MHz                |
| VCO Frequency                      |       |                                       | 300  |     | 1000 | MHz                |
| Feedback divider (programmable)    |       |                                       | 4  |     | 255  | Counts             |
| Output divider                     |       |                                       | /3 or /6   |     |      | Counts             |
| Additional output divider          |       |                                       | 1  |     | 64   | Counts             |
| Output clock duty cycle            |       | Only for even division @ o/p dividers | 50   |     |      | %                  |
|                                    |       | For odd output division               | 47   |     | 53   |                    |
| Frequency settling after power-up  |       | For 3 MHz divided reference           |  |     | 40   | μS                 |
| Jitter – accumulated long-term RMS |       |                                       |  | 40  |      | pS                 |
| Pk-pk Period jitter at PLL outputs |       |                                       |  |     | ±2   | % of output period |
| Power                              |       |                                       | Contact <a href="mailto:ip@cosmiccircuits.com">ip@cosmiccircuits.com</a> |     |      |                    |
| Die-Area                           |       |                                       | Contact <a href="mailto:ip@cosmiccircuits.com">ip@cosmiccircuits.com</a> |     |      |                    |
| Process                            |       |                                       | TSMC 65nm LP 6LM 2.5V IO   |     |      |                    |
| Status                             |       |                                       | GDS available  |     |      |                    |

**Note-1:** Product specifications are subject to change without notice. No responsibility is assumed for use of information herein.

**Note-2:** Products specifications such as that described above can typically be altered and customized for specific applications. Contact Cosmic Circuits for more information.

## ABOUT COSMIC CIRCUITS

Cosmic Circuits is a provider of differentiated and complex Analog, Mixed-Signal & RF Silicon IP cores. We create and provide IP cores that are best-in-class and thereby make our customers' solutions differentiated and low-cost.

Cosmic Circuits has quickly grown to be a company with the potential to become the destination of choice for world-wide customers for their complex and differentiated Analog, Mixed-Signal & RF Intellectual Property needs.

## DIFFERENTIATED IPS

We endeavor to create and provide Analog-IP solutions that are unique in functionality, burn the least amount of power, and take up minimal silicon die-area. 'Best-in-Class' is our Mantra. By using our analog-IP cores, our customers can expect their solution not to be disadvantaged because of analog, and even better, let the analog stand-out as a differentiating factor for the entire solution.

We value our unique blend of deep and broad analog skills and understanding of systems. Our customers can engage with our experts on the type of customization that needs to be done, or the kind of trade-offs to make, and expect the interaction to be a rewarding experience.

## DELIVERABLES

We provide the following deliverables to aid quick and reliable integration into the design flow. Please contact us for any additional views.

- ✓ GDSII
- ✓ Netlist (Spice format for LVS)
- ✓ Footprint (LEF format)
- ✓ User documentation
- ✓ Module integration guidelines
- ✓ Datasheet
- ✓ Silicon validation report (where available)
- ✓ Evaluation board (where available)

## LICENSING AND CUSTOMIZATION

Our engagements-models includes single-use and multi-use licensing of our IP-cores, Customization of IP-cores, Process porting of the cores to the customers' target process, turn-key development and licensing of customized IP cores and full-chip solutions, as well as supply of Known-Good-Dies (KGD) of full-chip ICs.

## SUPPORT

We consider ourselves successful when our customers succeed. We offer active support, both during the chip integration phase and during the product-ramp phase. We offer on-site support when needed. With Cosmic Circuits, our customers can be assured of a reliable partner interested in the success of the end product.

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